PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	)	
	)	
FREDERIC REBLEWSKI ET AL.	)	GROUP ART UNIT: 2123
	)	
DIV. OF SERIAL NO.: 09/404,920	)	EXAMINER: W.D. THOMSON
	)	
FILED: HEREWITH	)	
	)	ATTY. DKT. NO. 003921.00178
FOR: A REGIONALLY TIME MULTIPLEXED EMULATION SYSTEM	)	

INFORMATION DISCLOSURE STATEMENT

Commission for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with Applicants' duty of disclosure, the enclosed information is submitted to the United States Patent and Trademark Office in connection with the above-identified application. The information is identified on the attached PTO Forms-1449.

This application relies, under 35 U.S.C. §120, on the earlier filing date of prior U.S. Application Serial No. 09/404,920 filed on September 24, 1999. The references identified on the attached Form PTO 1449 were submitted to and/or cited by the Patent and Trademark Office in these prior applications and, therefore, copies are not required to be provided in this application. See 37 C.F.R. Section 1.98(d).

The relevance of the four Japanese documents is set forth in the July 2, 2002 Office Action from the Japanese Patent Office (an English translation of this Office Action previously was submitted to the U.S. PTO). Further comment is deemed unnecessary at this time.

Applicant does not waive any right to take appropriate action to establish patentability over the listed documents should they be applied as references against the claims of the present application.

It is respectfully requested that the Examiner fully consider each of the documents, initial the enclosed Form PTO-1449 in the appropriate place to indicate that the document has been considered, and return a copy of the initialed form to the undersigned in accordance with MPEP Section 609.

Respectfully submitted,

By: _____
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Dated: September 24, 2003

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 003921.00178	SERIAL NUMBER Div. of 09/404,920
	APPLICANT Frederic Reblewski et al.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE September 24, 2003	GROUP ART UNIT Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	5,363,319	11/1994	Okuda			
	5,574,388	11/1996	Barbier et al.			
	5,596,742	01/1997	Agarwal et al.			
	5,761,484	06/1998	Agarwal et al.			
	5,777,489	07/1998	Barbier et al.			
	5,847,578	12/1998	Noakes et al.			
	5,854,752	12/1998	Argarwal			
	5,920,712	07/1999	Kuijsten			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	
	WO 94/06210	03/1994	PCT				
	WO 94/23389	10/1994	PCT				
	04-138569	05/1992	Japan				
	08-030653	02/1996	Japan				
	08-508599	10/1996	Japan				
	11-073440	03/1999	Japan				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Babb et al., "Logic Emulation with Virtual Wires", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 6, pgs. 609-626, June 1997.
	Translation of an Office Action of Japanese Patent Office, " from a Japanese counterpart application, 7 pages, July 2, 2002.
	Office Action of Japanese Patent Office, from a Japanese counterpart application, 6 pages, July 2, 2002.
	Berger, "Teramac HW Simulator System External Reference Specification," November 7, 1991, Revision 1.1, pp. 3-37.
	Snider et al., "The PLASMA Chip Specification," August 1, 1995, pp. 1-124.
	Snider et al., "The Teramac Configurable Compute Engine," Field Programmable Logic and Applications, 5th International Workshop, FPL '95 Oxford, United Kingdom, pp. 44-53.
	XILINX, "The Programmable Gate Array Design Handbook," First Edition , 1986, pp. i-A-10.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 003921.00178	SERIAL NUMBER Div. of 09/404,920
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	4,642,487	02/1987	Carter			
	4,758,985	07/1988	Carter			
	5,036,473	07/1991	Butts			
	5,140,193	08/1992	Freeman, deceased et al.			
	5,701,441	12/1997	Trimberger, Stephen M.	326	39	
	5,943,490	08/1999	Sample			
	5,960,191	09/1999	Sample et al.	703	23	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Shibata, Y.; Miyazaki, H.; Xiao-Ping Ling; Amano, H., "Towards the realistic "virtual hardware," Innovative Architecture for Future Generation High-Performance Processors and Systems, 1997, 1998 pages: 50-55.
	Varghese, J.; Butts, M.; Batcheller, J., "An efficient logic emulation system," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume; 1 Issue: 2, June 1993 Pages: 171-174.
	Lo, W.Y.; Choy, C.S.; Chan, C.F., "Hardware emulation board based on FPGAs and Programmable Interconnections," Proceedings of the Fifth International Workshop on Rapid System Prototyping, 1994. Shortening the Path from Spec to Prototype. Pages 126-130.

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